The Section 103 Rejection

The Office Action asserts that:

In regards to claim 1, Kawai discloses the following:

a) one or more active substrates (l2a) comprising substantially transistors or diodes (l0) fonned thereon (For Example: See Figure 3 and Column 5 Lines 45 and 46);
b) one or more passive substrates (2a) comprising substantially inductors, capacitors or resistors (4) formed thereon (For Example: See Figure 3 and Column 4 Lines 17-20);
c) a plurality of bonding pads (15a and 5b) positioned on the active and passive substrates (For Example: See Figure 1); and
d) bonding wires (6) connected to the bonding pads (For Example: See Figure 1).

In regards to claim 1, Kawai fails to disclose the following:
a) a plurality of active substrates.
However, Riches discloses a semiconductor device that has a plurality of active substrates (For Example: See Page 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a plurality of active substrates as disclosed in Riches because it aids in providing a support for the interconnection of various components (For Example: See Page 1).
Additionally, since Kawai and Riches are both from the same field of endeavor, the purpose disclosed by Smiths would have been recognized in the pertinent art of Riches.
b) intra-substrate pads adapted to support wire-bonding within a substrate.
However, Tomura et a1. ("Tomura") discloses a semiconductor device that has intra-substrate pads adapted to support wire-bonding within a substrate (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include intra-substrate pads adapted to support wire-bonding within a substrate as disclosed in Tomura because it aids in providing interconnection (For Example: See Figure 1 and Abstract).
Additionally, since Kawai and Tomura are both from the same field of endeavor, the purpose disclosed by Tomura would have been recognized in the pertinent art of Kawai.

Applicants respectfully traverse the rejection. Kawai relates to a semiconductor device with a SAW device chip provided on a passive element chip in which a passive element circuit including a transmission line is formed on a semi-insulating compound substrate having one surface set to have a ground potential electrode.

Tomura shows a chip carrier with a carrier body including an upper face, a lower face, and an internal conductor; and a plurality of terminal electrodes formed on the upper face of the carrier body, the plurality of terminal electrodes electrically connecting an LSI chip to the internal conductor. A plurality of concave portions for electrically connecting a plurality of

electrodes on a circuit substrate to the internal conductor are provided on the lower face of the carrier body, the concave portions being electrically connected to the internal conductor. FIG. 1 of Tomura shows a chip package 19 with a multilayer ceramic chip carrier 12 and an LSI chip 7 mounted on the chip carrier 12 in a flip-chip fashion.

In Tomura, the LSI chip 7 includes a plurality of electrode pads 8 and projection electrodes 11 in such a manner that one projection electrode 11 is formed on each electrode pad 8... The electrode pads 8 and the projection electrodes 11 are used for connecting the wiring of an integrated circuit formed on the LSI chip 7 to an external circuit.. Each projection electrode 11 is electrically connected to one of a plurality of terminal electrodes 6 of the chip carrier 12 with a bonding layer (conductive adhesive) 9 interposed therebetween. The projection electrodes 11 preferably have a two-step convex shape (i.e. a shape consisting of one convex portion lying on top of another), so as to ensure a stable interconnection between the projection electrodes 11 and the terminal electrodes 6 of the chip carrier 12.

As shown above, Tomura's chip carrier assembly does not need wire-bonding and therefore Tomura fails to show the intra-substrate pads that allow wire bonding to be done within a substrate.

Further, as noted in paragraph 5 of the Wang declaration in the Pre-Appeal Brief, in the instant application, the intra-substrate pads and the wire-bonding among intra-substrate pads within a semiconductor IC such as the IC 20 are done to provide electromagnetic characteristics that are useful in certain radio frequency (RF) circuitry. For example, such intra-substrate wire-bonds can be used to vary resistance/capacitance/ inductance (RCL) characteristics useful for RF circuitry. Hence, the intra-substrate bonding on the IC is done to achieve a technical function that is different from the wiring for interconnection purposes of Kawai, Riches and Tomura as asserted in the Final Office Action.

Neither Kawai, Riches, nor Tomura shows as a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate.

As shown in FIG. 1 of the instant application, each substrate 20, 30 and 40 may have **intra-substrate pads that allow wire-bonding to be done within a substrate**.

Moreover, the combination of Kawai, Riches, and Tomura would result in an inoperable device. Riches disclose CMOS MCM substrates. Tomura discloses a chip carrier assembly. However, Tomura's chip carrier assembly technique would not work with IC dies having rough surface morphology such as the GaAs HBT IC that is used as the active die 20 in FIG. 1 of the instant application. One skilled in the art would not combine the dies of Kawai and Riches with the Tomura chip carrier because such a combination would not work.

Additionally, one skilled in the art would not have combined Kawaii, Riches and Tomura to arrive at active and passive IC modules with intra-substrate pads adapted to support wire-bonding within an IC substrate. As noted at http://www.microbonding.com/gb/fc_gb.htm, "flip chip technology is cheaper than wire bonding (true also with TAB) because bonding of all connections takes place simultaneously whereas with wire bonding one bond is made at a time." In this case, one skilled in the art would not have done a chip carrier and then wirebond two pads that are completely within an integrated circuit (IC) die. Combining the references as suggested by the Examiner would not be economical and one skilled in the art would not be motivated to combine as suggested as it is cheaper to provide interconnection using lines fabricated directly on the IC rather than to bond wires between pads on the IC.

The combination of CMOS and GaAs circuits would not provide performance WiFi circuits such as power amplifiers. Further, there is no motivation to combine soldering art used in Tomura's flip chip carrier with wirebonding of GaAs substrates. Hence, one skilled in the art would not combine Kawai with Riches or Tomura.

Applicant notes that the present rejection does not establish *prima facie* obviousness under 35 U.S.C. § 103 and M.P.E.P. §§ 2142-2143. The Examiner bears the initial burden to establish and support *prima facie* obviousness. *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976). To establish *prima facie* obviousness, three basic criteria must be met. M.P.E.P. § 2142. First, the Examiner must show some suggestion or motivation, either in the Kawai reference or in the knowledge generally available to one of

ordinary skill in the art, to modify the reference so as to produce the claimed invention. M.P.E.P. § 2143.01; *In re Fin*e, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Secondly, the Examiner must establish that there is a reasonable expectation of success for the modification. M.P.E.P. § 2142. Thirdly, the Examiner must establish that the prior art references teach or suggest all the claim limitations. M.P.E.P. §2143.03; *In re Royka*, 180 U.S.P.Q. 580 (CCPA 1974). The teachings, suggestions, and reasonable expectations of success must be found in the prior art, rather than in Applicant's disclosure. *In re Vaeck*, 20 U.S.P.Q.2d 1438 (CAFC 1991). Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on at least two of the above requirements.

Under *Vaeck*, absent any evidence of a cited suggestion or reasonable motivation in the Norand reference, or knowledge of those skilled in the art, *prima facie* obviousness of the independent claims (and those dependent therefrom) has not been established. As such, it is respectfully requested that the § 103(a) rejection of all claims be withdrawn and the claims be allowed.

Moreover, Kawai cannot render obvious any of the dependent claims that depend from allowable claim 1. First, as discussed above, the claims are allowable as none of the references show a device with a plurality of active substrates comprising substantially transistors or diodes formed thereon; one or more passive substrates comprising substantially inductors, capacitors or resistors formed thereon; a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate; and bonding wires connected to the bonding pads. Additionally, the references do not show the structures recited in the dependent claims. As the references fail to show a number of elements of the dependent claims, withdrawal of the Section 103 rejection on these claims is requested.

CONCLUSION

Applicants submit that all claims are in condition for allowance.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the undersigned at (408) 528-7490.

Respectfully submitted,

Bao Tran

Reg. No. 37,955